ABSTRACT OF THE DISCLOSURE

An improved analog to digital converter is disclosed incorporating a flash converter and a charge-sharing pipelined chain converter. The invention incorporates three important circuits including a novel voltage reference steering circuit, a novel high performance low power comparator circuit and a novel digital calibration for compensation circuit. The low power is accomplished by turning on compare circuits only when comparing (controlled by timing circuits that are common to all comparators) and by a low power RAM that properly aligns the converted data. The converter operates in a pipelined manor and requires multiple sample and hold circuits for the compare circuits. The improved analog to digital converter incorporates test and calibration to compensate for variations experience during operation and manufacture of the improved analog to digital converter.